ABSTRACT OF THE DISCLOSURE

A Content Addressable Memory (CAM) cell is presented which provides for improved speed and enhanced reliability. The CAM architecture enables maximal conduction of one of the output series pass transistors in the case of a data mismatch during a search operation thereby producing a minimal voltage drop, low impedance path for charging the bootstrap capacitance at the enabled output controlled switch, and causes one of the series pass transistors to conduct for discharging the bootstrap capacitance at the beginning of the precharge period of the bit lines.